Remarks/Arguments

ITEM 4

Claim Rejections – 35 USC 102(b):

Claims 1-8 stand rejected under 35 U.S.C. §102(b) as being anticipated by Yamashita (US6222323).

Applicant asserts that Yamashita does anticipate any of the claims and that Yamashita is not revelant to the claims, because the transfer of charges that is disclosed in columns 5 & 6 therein address the avoidance of any difference of stored charges in parasitic capacitance of cells to be lit, "due to the (potential) difference of bias status just before the lighting" (column 6, lines 1-4) . The drawback that Yamashita attempts to avoid is disclosed at column 1, lines 56-64. In contrast, the claimed invention in applicant's handles the transfer of charge in a different manner such that the transfer participates in the powering of the cells.

Claim 1

Claim 1 is directed to a device for displaying images comprising:
- an image display panel comprising a first array (column - anodes X) and a second array (row - cathodes Y) of electrodes which serve an array of cells (11), where each cell (11) may be powered between an electrode (column - anode) of the first array and an electrode (row - cathode) of the second array effecting between them an intrinsic capacitor Ci (specification at page 9, lines 22-27 and page 10, lines 22-23),
- power supply means for generating a potential difference between two terminals (see, specification at page 9,lines 29-31),
- drive means :

adapted for successively connecting each (row) electrode of the second array to one of the terminals of the power supply means (specification at page 9, lines 33-38).

adapted for, during each sequence of connection of a (row) electrode of the second array, simultaneously connecting one or more or even all the (column) electrodes of the first array to the other terminal of the power supply means in order to power the cell(s) linked both to this (row) electrode of the second array and this/these (column) electrodes of the first array (specification at page 9, lines 33-38"), and

adapted for being able, during said sequence of connection of an (row) electrode of the second array, to transfer to each of this/these cell(s) to be powered the charge of the intrinsic capacitors of the other cells that are linked to the same (column) electrode of the first array as the cell to be powered (see, specification at page 11, lines 37-39, 11-14, page 17, lines 17-29).

Yamashita discloses a device for displaying images comprising:

an image display panel (1) comprising a first array (column - anodes - 2) and a second array (row - cathodes - 5) of electrodes (Fig.2, col. 4, lines 39-54) which serve an array of cells (6), where each cell may be powered between an electrode (column - anode) of the first array and an electrode (row - cathode) of the second array effecting between them an intrinsic capacitor Ci (see, fig.5, col. 5, lines 15-25);

power supply means (current sources J1, J2 at col. 5, lines59-61);

voltage source Vcc for applying "reverse bias voltage" such that a potential difference between two terminals is generated (i.e. the two terminals are the J terminals on the anode (column) side, and the ground terminal on the cathode (row) side) (col. 5, lines 31-35);

drive means:

-adapted for successively connecting each (row) electrode of the second array to one of the terminals of the power supply means ("cathode controller" 8; Figs. 1 and 5-7 and col. 5, lines 1-32, wherein "couples cathode line c1 to ground potential" appears at col. 5, lines 30-31), and

-adapted for, during each sequence of connection of a (row) electrode of the second array, simultaneously connecting one or more or even all the (column) electrodes of the first array to the other terminal of the power supply means in order to power the cell(s) linked both to this (row) electrode of the second array

and this/these (column) electrodes of the first array (anode controller 7: Figs.1, 5-7 and col.5, lines 1-32, wherein "couple anode lines "a2-am" to current source J1" appears at col. 5, lines 29-30).

However, Yamashita fails to disclose a drive means that is "adapted for being able, during said sequence of connection of an (row) electrode of the second array, to transfer to each of this/these cell(s) to be powered the charge of the intrinsic capacitors of the other cells that are linked to the same (column) electrode of the first array as said cell to be powered," which is a key feature of the invention and generally recited in each of applicant's claims.

Rather, Yamashita in col. 5, line 15 col. 6, line 11 describes very precisely two successive sequences of connections of a (row) electrode of the second array to the ground, wherein there is transfer of charge. A first 1st sequence is when element L1,1 is illuminated and a 2nd sequence when L1,2 and L2,2 are illuminated. (col. 5, lines 24-25) Each sequence is characterized by the connection of a different (row) cathode electrode (c1, then c2) to one of the terminals of the power supply means (i.e. ground). Steps of Fig. 1, 5 and 6 belong to the 1st sequence. The step of Fig. 7 belongs to the 2nd sequence.

In Yamashita, during the steps of Fig. 1, 5 and 6 of the 1st sequence, switch Sc1 (of the "cathode controller" 8) couples the 1st cathode line c1 to ground potential with no change to the position of the switch Sc1 in figure 5 and 6. (col. 5, lines 30-31) During the 1st step (**Fig.1**) of the 1st sequence (col. 5, **lines 28-38**) only one (column) anode electrode (a1) of the first array is connected (via the switch Sa1) to the (other) terminal of the power supply means J1 (see col.5, lines 28-29) in order to **power** the cell L1,1 linked both to the (row) cathode electrode (c1) of the second array and this (column) electrode (a1) of the first array. Charges are stored on the parasitic capacitance associated with the cells not to be powered "placed at the intersections of anode lines "a2-am" and cathode lines "c2-cn."" (see column 5, lines 33-35)

More specifically, during a 2nd step (**Fig. 5-6**) of the 1st sequence in Yamashita (col. 5, **lines 39-58**) on column anode line a1, having a cell to power during the 1st sequence (L1,1) (and likewise in the 2nd sequence (see below: L1,2)). charges stored therein are discharged. This is contrary to the invention, because charge is not transferred to another cell as the cell L1,2 of the same column anode line a1 to be powered during the 2nd sequence.

Further in Yamashita (col. 5, **lines 39-58**), on column anode line a2, having a cell to power during the 2nd sequence (see below: L2,2), charges stored in cells "L2,2-L2,n" discharge. This too is **contrary to the invention**, because charge is not transferred to another cell as the cell L2,2 of the same column anode line a2 to be powered during the 2nd sequence (see below).

Also in Yamashita (col. 5, **lines 39-58**) on column anode line a3 (having **no cell to power** during subsequent sequences), charge stored in cells "L3,2-L3,n" moves (partially) to cell L3,1. This too is **contrary to the invention**, because this charge is not used to power any cell linked to the same (column) electrode during any subsequent sequences.

In Yamashita during the step of Fig. 7 of the 2nd sequence, switch Sc2 (of the "cathode controller" 8) couples the 2nd cathode line c2 to ground potential. (col. 5, lines 63-64) Similarly to the 1st step of the 1st sequence, during the 1st step (**Fig.7**) of **the 2nd sequence (col. 5, lines 59 – col. 6, line 11)**, two (column) anode electrodes (a1, a2) of the first array are connected (via the switches Sa1, Sa2) to the (other) terminal of the power supply means J1, J2 (see col.5, lines 60-61) in order to **power** the cells L1,2 and L2,2 linked both to the (row) cathode electrode (c2) of the second array and these (column) electrodes (a1, a2) of the first array. The charges are stored on the parasitic capacitance associated with the cells not to be powered "L3,1-Lm,1" (i.e. cells of row c1), "L3,3-Lm,3" (i.e. cells of row c3). "L3,4-Lm,4" (i.e. cells of row c4), ..., "L3,n-Lm,n" (i.e. cells of row cn) placed at the intersections of anode lines "a3-am" and cathode lines c1 and "c3-cn" (see column 6, lines 8-10). Moreover, the stored charges in cells L3,2-Lm,2 (i.e. cells not to be powered of row c2) discharges slightly (of an amount [(n-1)/n].Q). (col. 6, lines 5-8)

As demonstrated above, the only **transfer of charges** which is mentioned in Yamashita concern items concerns the 2nd step of the 1st sequence (see the wording : "charges ... move ... to"). However, Yamashita does not disclosed that, during a sequence of connection of an (row) electrode of the second array, a transfer of charges occur toward each of the cell(s) to be **powered** of this (row) electrode from the intrinsic capacitors of the other cells that are linked to the same (column) electrode as the cell to be powered. Consequently, the last feature of claim 1 is not disclosed by Yamashita et al. Consequently, claim 1 is not anticipated by Yamashita.

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Claim 2

Claim 2 which depends on claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita. Applicant asserts that this claim is not anticipated by Yamashita.

Claim 2 is directed to the following additional feature: the drive means are adapted so that, during each sequence of connection of an electrode of the second array, the transfer of charge via each of the (column) electrodes of the first array is favored at the expense of the connection of these (column) electrodes to said power supply means. Contrary to what is asserted in the office action, col.5, lines 39-58 referring to Fig.5-6 (i.e. the 2nd step of the 1st sequence described above) in Yamashita does not disclose such a feature, because the only transfer of charge which is mentioned in this excerpt (see the wording above : "charges ... move ... to") has no influence on the connection of the (column) electrodes to the power supply means (J1, J2, J3, ..., Jm) via the switches Sa1, Sa2, Sa3, ..., Sam of the driving means ("anode controller 7").

Consequently, claim 2 is not anticipated by Yamashita.

Claim 3

Claim 3 which depends on claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita. Applicant asserts that this claim is not anticipated by Yamashita.

Claim 3 is directed to the following additional feature: each image to be displayed is divided into pixels or subpixels to which are allocated luminous intensity data, each cell of the panel being assigned to a pixel or subpixel of the images to be displayed, the device for displaying images comprises means of processing said data so as to be able, **during** each sequence of connection of an (row) electrode of the **second** array, to **modulate the duration of connection** t'_{a1} of each (column) electrode of the **first array** to said power supply means and to **modulate the duration** of **said transfer of charge t'_{a2} of the intrinsic capacitors** of the other cells linked to the same (column) electrode of the first array, as a function of the luminous intensity datum of the cell that has to be **powered** between this electrode of the first array and this electrode of the second array. However, Yamashita does not disclose (see detailed analysis

of Yamashita concerning claim 1) any transfer of charge from the intrinsic capacitors of the cells linked a (column) electrode toward a cell to power that is linked to the same (column) electrode (see claim 1 to which claim 3 depends).

Consequently, claim 3 is not anticipated by Yamashita.

Claim 4

Claim 4 which depends on claim 3 stands rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita. Applicant asserts that this claim is not anticipated by Yamashita.

Claim 4 is directed to the adaptation of the drive means so that, during each **sequence** of connection of an (row) electrode of the second array, said connection of each (column) electrode of the first array to said power supply means is carried out, as appropriate, at the end of a However, the only transfer of charge which is disclosed in Yamashita et al. concerns the 2nd step (i.e. the end, but not the start as in the invention) of a sequence of connection of an (row) electrode of the second array (see the 1st sequence in the detailed analysis of Yamashita et al. above, concerning claim 1).

Consequently, claim 4 is not anticipated by Yamashita.

Claims 5-8

Claims 5-8 each ultimately depend on claim 1 and stand rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita. However, because claims 5-8 include the features of claim 1, Applicant asserts that the claims 5-8 are also not anticipated by Yamashita in light of the same reasons advanced by applicant for claim 1.

ITEM 6

Claim 9

Claim 9 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. (US 6,222,323) in view of Aziz et al. (US 6,811,896).

Claim 9 depends on claim 8 and ultimately depends on claim 1.

Claim 1 is directed to a device for displaying images comprising:

- an image display panel comprising a first array (column - anodes X) and a second array (row - cathodes Y) of electrodes which serve an array of cells (11), where each cell (11) may be powered between an electrode (column - anode) of the first array and an electrode (row - cathode) of the second array effecting between them an intrinsic capacitor Ci (specification at page 9, lines 22-27 and page 10, lines 22-23),
- power supply means for generating a potential difference between two terminals (see, specification at page 9,lines 29-31),
- drive means :

adapted for successively connecting each (row) electrode of the second array to one of the terminals of the power supply means (specification at page 9, lines 33-38),

adapted for, during each sequence of connection of a (row) electrode of the second array, simultaneously connecting one or more or even all the (column) electrodes of the first array to the other terminal of the power supply means in order to power the cell(s) linked both to this (row) electrode of the second array and this/these (column) electrodes of the first array (specification at page 9, lines 33-38"),

adapted for being able, during said sequence of connection of an (row) electrode of the second array, to transfer to each of this/these cell(s) to be powered the charge of the intrinsic capacitors of the other cells that are linked to the same (column) electrode of the first array as said cell to be powered (see, specification at page 11, lines 37-39, 11-14, page 17, lines 17-29), and

- an organic electroluminescent layer having a thickness of less than or equal to 0.2 μm.

Yamashita discloses a device for displaying images comprising:

an image display panel (1) comprising a first array (column - anodes - 2) and a second array (row - cathodes - 5) of electrodes (Fig.2, col. 4, lines 39-54) which serve an array of cells (6), where each cell may be powered between an electrode (column - anode) of the first array and an electrode (row - cathode) of the second array effecting between them an intrinsic capacitor Ci (see, fig.5, col. 5, lines 15-25);

power supply means (current sources J1, J2 at col. 5, lines59-61);

voltage source Vcc for applying "reverse bias voltage" such that a potential difference between two terminals is generated (i.e. the two terminals are the J terminals on the anode (column) side, and the ground terminal on the cathode (row) side) (col. 5, lines 31-35);

drive means:

-adapted for successively connecting each (row) electrode of the second array to one of the terminals of the power supply means ("cathode controller" 8; Figs.1 and 5-7 and col. 5, lines 1-32, wherein "couples cathode line c1 to ground potential" appears at col. 5, lines 30-31), and

-adapted for, during each sequence of connection of a (row) electrode of the second array, simultaneously connecting one or more or even all the (column) electrodes of the first array to the other terminal of the power supply means in order to power the cell(s) linked both to this (row) electrode of the second array and this/these (column) electrodes of the first array (anode controller 7: Figs.1, 5-7 and col.5, lines 1-32, wherein "couple anode lines "a2-am" to current source J1" appears at col. 5, lines 29-30).

Aziz discloses "the luminescent region between the anode and cathode electrodes of the OLED" to be "usually less than 200 nm thick." (col. 1, line 56-58)

However, Yamashita and Aziz separately and in combination fail to disclose a drive means that is "adapted for being able, during said sequence of connection of an (row) electrode of the second array, to transfer to each of this/these cell(s) to be powered the charge of the intrinsic capacitors of the other cells that are linked to the same (column) electrode of the first array as said cell to be powered," which is a key feature of the invention and generally recited in each of applicant's claims.

Therefore, claim 9 is not made obvious by Yamashita.in view of Aziz. As such, reconsideration of the rejection to claim 9 is requested.

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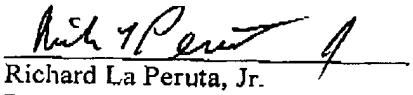
Conclusion

In light of the above assertions, reconsideration of the rejections to each of the claims is respectfully requested.

If the Examiner has any questions or comments that would facilitate the disposition or resolution of the issues, he is respectfully requested to contact the undersigned at 609-734-6816.

Respectfully submitted,
Jean-Paul Dagois, Applicant



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